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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/982,242	10/16/2001	Karthisha S. Canagasaby	042390.P11916X	8029

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EXAMINER	
LUU, CUONG V	
ART UNIT	**PAPER NUMBER**
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/982,242	CANAGASABY ET AL.	
	Examiner	Art Unit	
	Cuong V. Luu	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 5-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2 and 5-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-2 and 5-30 are pending. Claim 4 has been canceled. Claims 1-2 and 5-30 have been examined. Claims 1-2 and 5-30 have been rejected.

Response to Arguments

1. Applicant's arguments filed 1/22/2007 have been fully considered but they are not persuasive. The Applicant argues that Puri discloses estimating the output slew of the output waveform from the input slew of the input waveform of the same RC circuit, not creating a second graphical presentation of an output of the test network that approximates the first graphical representation of the output of the interconnection within a specified tolerance as recited in the amended claim 1. The Examiner respectfully disagrees. In figure 4, figure 6, step 680, and col. 7 lines 61-67, Puri teaches creating a second graphical representation of the output of the RC test network that approximates the first graphical representation of the output of the interconnection within a specified tolerance. It would have been obvious to one of ordinary skill in the art to combine the teachings of Muddu and Puri. Puri's teachings would have yielded more accurate delays for both the interconnects and source driver (the abstract). The amended claim 1, therefore, is rejected.

2. As per claims 2 and 5-30, the Applicant argues that they contain similar limitations; therefore, they are allowable. Since claim 1 is rejected as discussed in item 1, claims 2 and 5-30 stay rejected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-2 and 5-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muddu (U.S. Patent 6,314,546 B1) in view of Puri et la, herein Puri, (U.S. Patent 6,601,223 B1).

1. As per claim 1, Muddu teaches a method comprising:

   measuring first electrical characteristics of an interconnection, including generating a first graphical representation of an output of interconnection that is based, at least in part, on the first electrical characteristics (the abstract, lines 22-28; col. 7, lines 14-22. In this portion of the abstract, Muddu teaches generating graphical representation of an output of interconnection and measuring its characteristics. Muddu also teaches measuring rise or fall

time which is the first electrical characteristics of an interconnection in col. 7, lines 14-22); and

determining a test network having second electrical characteristics such that the first electrical characteristics of the interconnection are approximated by the second electrical characteristics of the test network, wherein determining the test network includes adjusting the second characteristics based on the first graphical representation (col. 5, lines 12-31. In these lines, Muddu teaches determining a test network; capacitive, resistive, or combination; such that the first electrical characteristics of the interconnection are approximated by the second electrical characteristics of the test network, which is the delay time and the calculating or adjusting of this second characteristics is based on the calculation resulted from the first characteristics, rise or fall time).

Muddu does not teach approximating by the second electrical characteristics of the test network within a specified tolerance nor creating a second graphical representation of an output of the resistive/capacitive network that approximates the first graphical representation of the output of the interconnection within a specified tolerance.

Puri teaches these features (figure 4, figure 6, step 680, and col. 7 lines 61-67).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Muddu and Puri. Puri's teachings would have yielded more accurate delays for both the interconnects and the source driver (the abstract).

2. As per claim 5, Puri teaches a specified tolerance, as discussed in claim 1, but does not specifically teach the tolerance of 10%. This number of 10% is a design choice. It would have been obvious to one of ordinary skill in the art to select a specified tolerance of any number including 10%.

3. As per claim 6, Muddu teaches the test network is a resistive network (col. 4, lines 45-48).

4. As per claim 7, Muddu teaches the test network is a capacitive network (col. 4, lines 45-48).

5. As per claim 8, Muddu teaches the test network is comprised of a plurality of resistive/capacitive networks (col. 4, lines 45-48).

6. As per claim 9, Muddu teaches connecting the resistive/capacitive network between a driver of a first input/output circuit and a receiver of a second input/output circuit (Fig. 1. This figure shows interconnect modeled with resistive/capacitive network connected between a driver and receiver).

7. As per claim 10, these limitations have already been discussed in claim 9. They are, therefore, rejected for the same reasons.

8. As per claim 11, variable resistors and capacitors have existed for decades. It would have been obvious to one of ordinary skill in the art to use them to implement a resistive/capacitive network in order to vary their values to approximate the interconnect.

9. As per claim 12, Muddu teaches the resistive/capacitive network is implemented on an integrated circuit chip (col. 1, lines 18-25).

10. As per claim 13, it is well known to one of ordinary skill in the art a capacitor is can be implemented with gate capacitance. Therefore, it would have been obvious to one of ordinary skill in the art to use distributed gate capacitance to implement the capacitance.

11. As per claim 14, it is well known to one of ordinary skill in the art to implement the resistive/capacitive network on a printed circuit board. It would have been obvious to one of ordinary skill in the art to implement the resistive/capacitive network on a printed circuit board.

12. As per claim 15, Muddu teaches an apparatus comprising:

an integrated circuit having at least one input/output ports, the at least one input/output ports having a driver and a receiver (col. 1, lines 13-15. An integrated circuit inherently have at least one input/output ports having a driver and a receiver); and

a test network having second electrical characteristics, the test network electrically coupling the driver and the receiver such that an input/output interface interconnection having first electrical characteristics may be emulated therewith, wherein the second electrical characteristics are adjusted based on a first graphical representation of an output of the input/output interface interconnection that is generated based, at least in part, on the first electrical characteristics, wherein an output of the test network generates a second graphical representation of that approximates the first graphical representation of the output of the input/output interface interconnection (these limitations have already been discussed in claim 1).

13. As per claim 16, these limitations have already been discussed in claim 2. They are, therefore, rejected for the same reasons.

14. As per claim 17, these limitations have already been discussed in claim 6. They are, therefore, rejected for the same reasons.

15. As per claim 18, these limitations have already been discussed in claim 7. They are, therefore, rejected for the same reasons.

16. As per claim 19, these limitations have already been discussed in claim 11. They are, therefore, rejected for the same reasons.

17. As per claim 20, these limitations have already been discussed in claim 12. They are, therefore, rejected for the same reasons.

18. As per claim 21, these limitations have already been discussed in claim 14. They are, therefore, rejected for the same reasons.

19. As per claim 22, a microprocessor is a big integrated circuit comprising of many smaller blocks of integrated circuits. Therefore, the examiner interprets that the integrated circuit is part of a microprocessor.

20. As per claim 23, these limitations have already been discussed in claim 15. They are, therefore, rejected for the same reasons.

21. As per claim 24, these limitations have already been discussed in claim 2. They are, therefore, rejected for the same reasons.

22. As per claim 25, these limitations have already been discussed in claim 1. They are, therefore, rejected for the same reasons11.

23. As per claim 26, these limitations have already been discussed in claim 8. They are, therefore, rejected for the same reasons.

24. As per claim 27, Muddu teaches the capacitive elements are distributed RC ladder (col. 4, lines 40-45; col. 5, lines 17-34).

25. As per claim 28, these limitations have already been discussed in claim 20. They are, therefore, rejected for the same reasons.

26. As per claim 29, these limitations have already been discussed in claim 14. They are, therefore, rejected for the same reasons.

27. As per claim 30, these limitations have already been discussed in claim 1. They are, therefore, rejected for the same reasons.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cuong V. Luu whose telephone number is 571-272-8572. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah, can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. An inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group receptionist: 571-272-2100.

FRED FERRIS
PRIMARY EXAMINER
TECHNOLOGY CENTER 2100